Memory and Programmable Logic

Memory Device:

Device to which binary information is transferred for storage, and from which information is available for processing as needed.

Memory Unit:

is a collection of cells capable of storing a large quantity of binary information.

In digital systems, there are two types of memories:

1. RAM
2. ROM

Memory and Programmable Logic

1. *Random-Access Memory* (RAM)

RAM is the place in a computer where the operating system , application programs, and data in current use are kept so that they can be quickly reached by the computer's processor.

2. *Read-Only Memory* (ROM):

ROM is a type of memory that is as fast as RAM, but has two important differences: It can not be changed, and it retains its contents even when the computer is shut off. It is generally used to start your computer up and load the operating system.

Using a ROM as a PLD: A programmable logic device or PLD is an electronic component used to build digital circuits . Before the PLD can be used in a circuit it must be programmed.

Examples of PLDs: programmable logic array (PLA), programmable array logic (PAL), and *field-programmable logic gate array* (FPGA). (PAL: Program. AND, fixed OR, PLA: Program. AND/OR)

Random-Access Memory

Memory unit:
Stores binary information in groups of bits called *words*.

Memory word:
group of 1's and 0's and may represent a number, character(s), instruction, or other binary-coded information.

Most computer memories use words that are multiples of 8 bits (*byte*).
32-bit word → 4 bytes

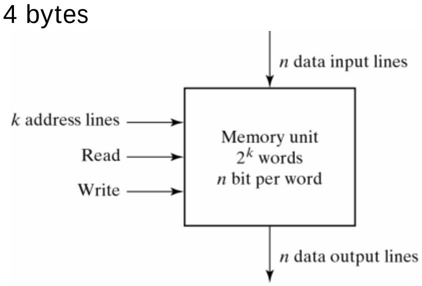


Fig. 7-2 Block Diagram of a Memory Unit

Random-Access Memory

Each word in memory is assigned an address 0 up to $2^k - 1$ (k = # of address lines).

Memory address		Memory contest / memory content
Binary	decimal	
0000000000	0	
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

How many bytes is this memory module? 2KB

RAM: Write and Read Operations

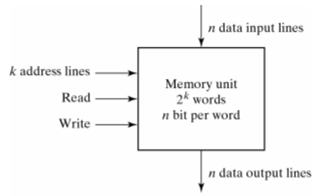


Fig. 7-2 Block Diagram of a Memory Unit

To transfer a new word to be stored into memory:

1. Apply the binary address of the word to address lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the *write* input.

To transfer a stored word out of memory:

1. Apply the binary address of the word to address lines.
2. Activate the *read* input.

Memory Types

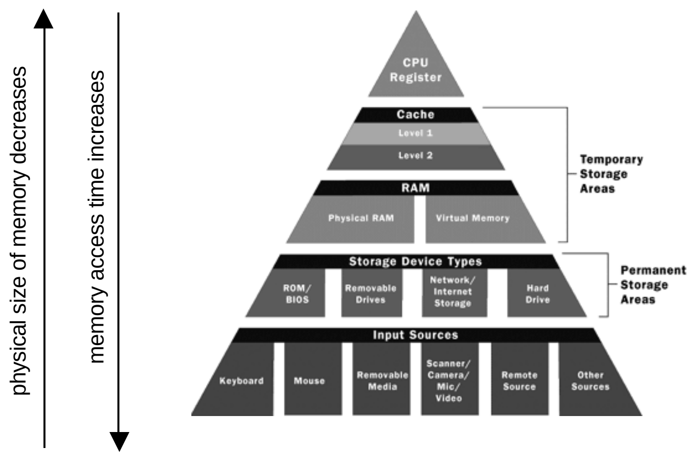
Integrated circuit RAM units are available in two possible operating modes: *static* and *dynamic*.

Static RAM **(SRAM)** consists of of internal latches that store the binary information. The stored information remains valid as long as power is applied to the unit.

Dynamic RAM **(DRAM)** stores the binary information in the form of electric charges on capacitors provided by the MOS transistors.
The charge on the capacitors tends to decay with time and the capacitors must be periodically recharged by *refreshing* of the dynamic memory every few milliseconds.

• DRAM offers reduced power consumption, large integration of units on chip.
• SRAM is faster; has shorter read and write cycles, SRAM is used in cache.
Disadvantages: high power consumption, low density, expensive.

Memory Hierarchy



Volatile vs. Non-Volatile Memory

- RAM (static and dynamic) is said to be volatile, since information is lost when power is turned off.
- Non-volatile memory retains its information even when power is turned off.

1. Magnetic disks: stored data is represented by the direction of magnetization.
2. CD: compact disc is a piece of polycarbonate (a type of plastic) on which a spiral track has been impressed. This spiral track is a series of indentations ("pits") separated by flat areas ("land").
3. ROM: The internal storage elements are set to their values once and after that are only read.

EPROMS and PROMS

Erasable Programmable Read-Only Memory **(EPROM)** is a special type of memory that retains its contents until it is exposed to ultraviolet light.

To write to EPROM, you need a special device called a *PROM Programmer* or *PROM burner (programmer).* An EPROM differs from a PROM in that a PROM can be written to only once and cannot be erased.

EPROMs are widely used in personal computers since they enable the manufacturer to change the contents of the PROM before the computer is actually shipped. This means that bugs can be removed and new versions installed shortly before delivery.

EEPROMS and FLASH

Electrically Erasable Programmable Read-Only Memory **(EEPROM),** is like EPROM except that the previously programmed connections can be erased with an electrical signal.

Flash memory is a type of EEPROM. Information stored in flash memory is usually written in blocks rather than a byte or word at a time.

Virtual Memory?
With virtual memory, the computer can look for areas of RAM that have not been used recently and copy them onto the hard disk. This frees up space in RAM to load the new application. Because it does this automatically, you don't even know it is happening, and it makes your computer feel like is has unlimited RAM space even though it has only 1 GB installed.

RAM Memory Cell

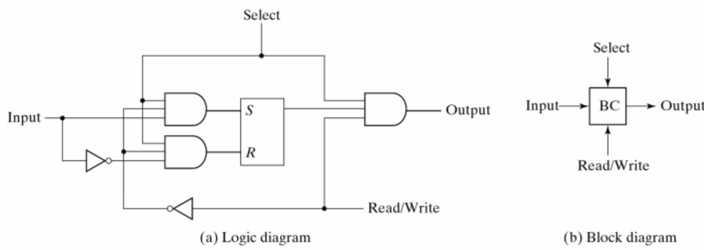


Fig. 7-5 Memory Cell

The storage part of the cell is modeled by an *SR* latch with associated gates.

A 1 in the read/write input provides the read operation by forming a path from the latch to the output.
A 0 in the read/write input provides the write operation by forming a path from the input to latch.

4 x 4 RAM

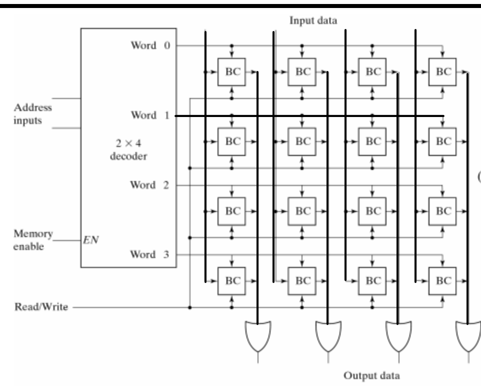


Fig. 7-6 Diagram of a 4 × 4 RAM

Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

WRITE operation: the data available in the input lines are transferred into the four binary cells of the selected word. The memory cells that are not selected are disabled.
READ Operation: the four bits of the selected word go through OR gates to the output terminals.

Commercial RAM

Commercial RAM → thousands of words, with each word 1 - 64 bits.
A memory with 2^k words of n bits/word requires k address lines that go into a k x 2^k decoder.

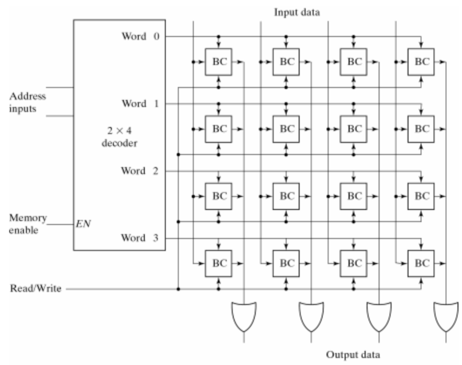


Fig. 7-6 Diagram of a 4 × 4 RAM

Two Dimensional Decoding

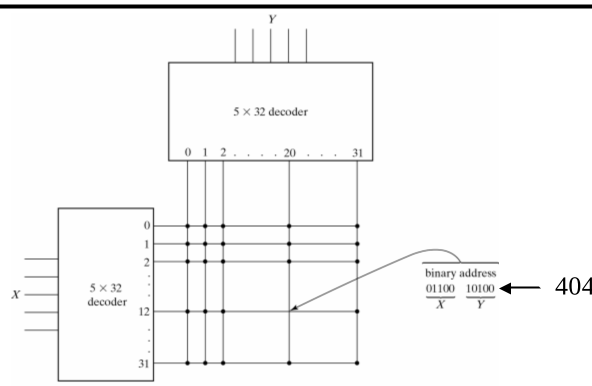


Fig. 7-7 Two-Dimensional Decoding Structure for a 1K-Word Memory

The idea of two-dimensional decoding is to arrange the memory cells in an array that is as close as possible to square. Use two $k/2$-input decoders instead of one k-input decoder. One decoder performs the row selection and the other the column selection in a two dimensional matrix configuration.
How many words can be selected?

Read-Only Memory (ROM)

Read-only memory is a memory device in which permanent binary information is stored.

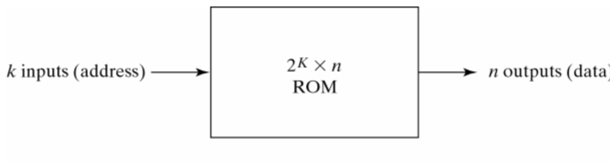


Fig. 7-9 ROM Block Diagram

• The number of words in a ROM is determined from the *k* address input lines needed to specify the 2^k words.

• **Why doesn't the ROM have any data inputs?**

Read-Only Memory (ROM)

A 32 x 8 ROM consists of 32 words of 8 bits each. The five input lines are decoded by into 32 distinct outputs (memory addresses) using a 2^5 x 8 decoder. Each OR gate has 32 input connections → 32 x 8 ROM has internal connections 32 x 8.
In general, a 2^k x *n* ROM will have *k* x 2^k decoder and *n* OR gates with 2^k x *n* internal connections.

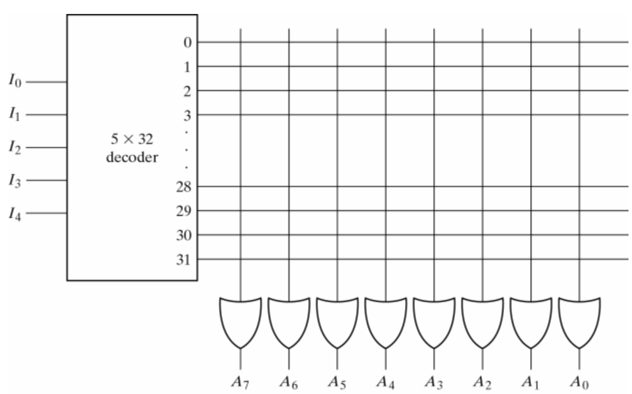


Fig. 7-10 Internal Logic of a 32 × 8 ROM

Read-Only Memory

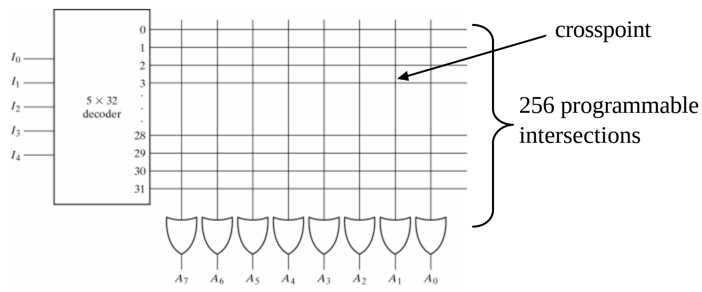


Fig. 7-10 Internal Logic of a 32 × 8 ROM

A programmable connection (a crosspoint) between two lines is logically equivalent to a switch that can be be closed (two lines are connected) or open (two lines are disconnected). A switch can be a fuse that normally connects the two points, but can be opened by blowing the fuse using a high voltage pulse.

Programming Read-Only Memory

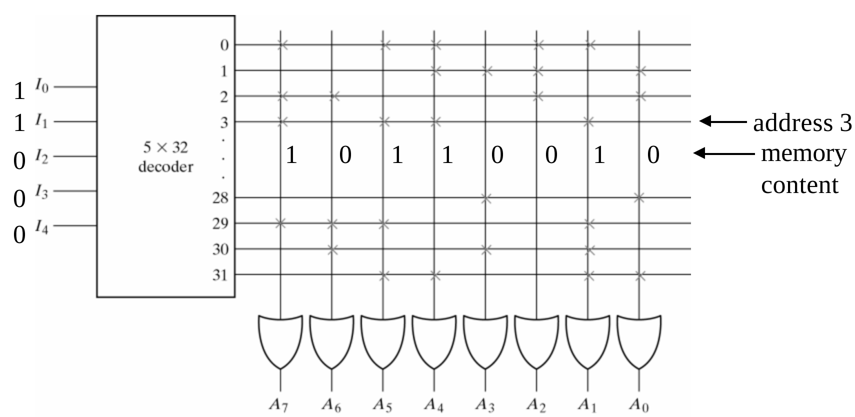


Fig. 7-11 Programming the ROM According to Table 7-3

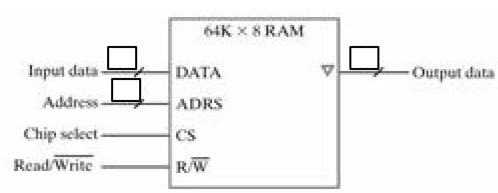
Output A_6 can be expressed in sum of minterms as: $A_6(I_4, I_3, I_2, I_1, I_0) = \Sigma(2, ..., 29, 30)$

Constructing 256K X 8 RAM (similar to 7-8)

1. How many 64K x 8 RAM chips are needed to provide a memory capacity of 256KB?
2. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
3. How many lines must be decoded for the chip select inputs of all chips?

64K X 8 RAM chip

Capacity: 64K words of 8 bits each



How many chips are needed to construct 256K x 8?
What is the size of the decoder?

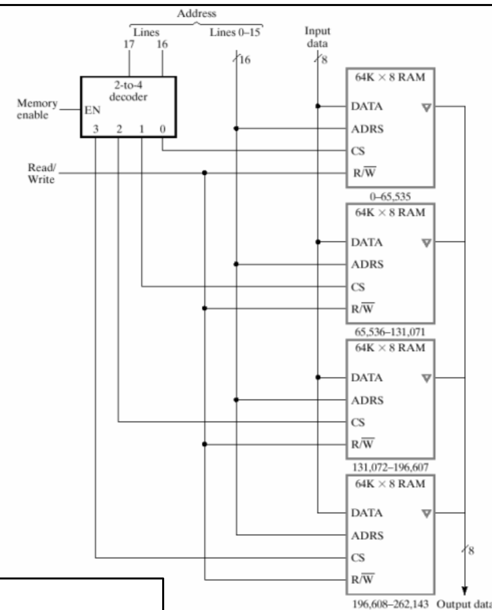
256K X 8 RAM

- Three-state outputs are connected together to form 8 data output lines.

- Just one chip select (CS) will be active at any time.

- RAM requires 18-bit address:
16 LSB address are applied to the inputs of each RAM.
2 MSB are applied to 2-to-4 decoder.

- Address bits 16 and 17 are used for chip selection.



32 X 8 ROM chip

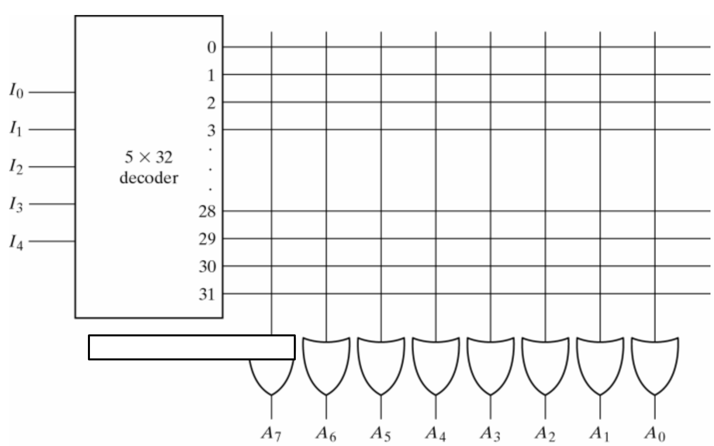
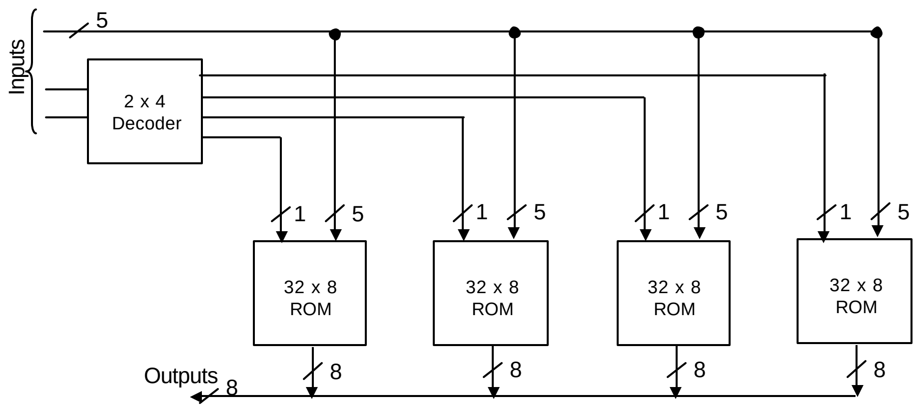


Fig. 7-10 Internal Logic of a 32 × 8 ROM

128 X 8 ROM chip (similar to 7-15)



Programmable Logic Device (PLD)

Programmable logic devices (PLD) are designed with configurable logic and flip-flops linked together with programmable interconnect.

PLDs provide specific functions, including
- Device-to-device interfacing
- Data communication
- Signal processing
- Data display
- Timing and control operations, and almost every other function a system must perform

PLDs (continued)

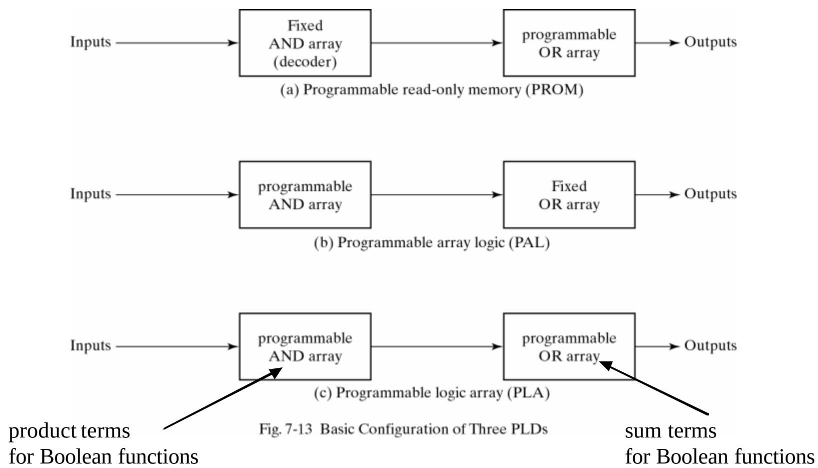


Fig. 7-13 Basic Configuration of Three PLDs

Programmable Logic ARRAY (PLA)

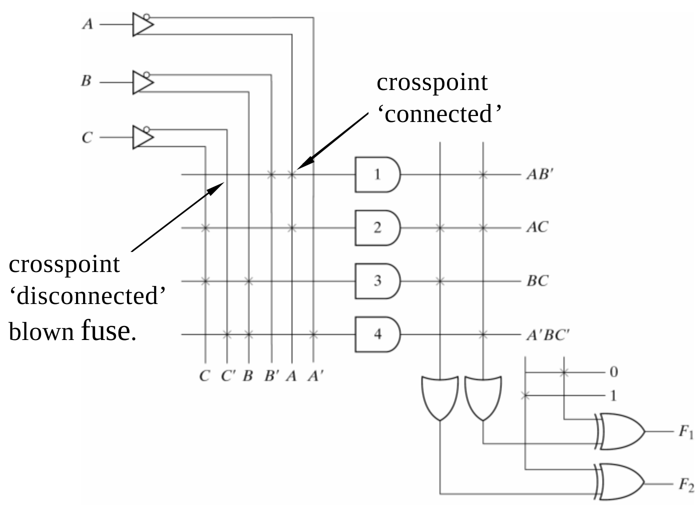


Fig. 7-14 PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

PLA Programming Table

	product term	Inputs A	B	C	Outputs F_1	F_2
AB'	1	1	0	-	1	-
AC	2	1	-	1	1	1
BC	3	-	1	1	-	1
$A'BC'$	4	0	1	0	1	-

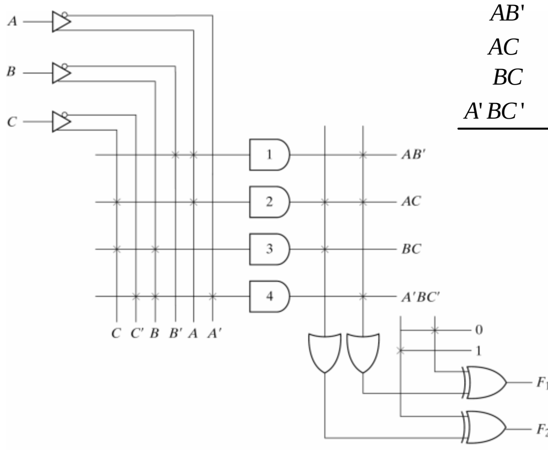


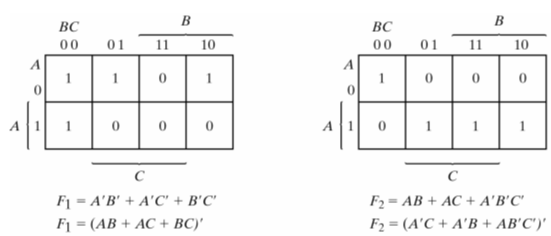
Fig. 7-14 PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

PLA Programming example

Implement the following function with a PLA:

$F_1 = \Sigma(0,1,2,4)$

$F_2 = \Sigma(0,5,6,7)$



PLA programming table

	Product term	Inputs A	B	C	Outputs (C) F_1	(T) F_2
AB	1	1	1	–	1	1
AC	2	1	–	1	1	1
BC	3	–	1	1	1	–
$A'B'C'$	4	0	0	0	–	1

Fig. 7-15 Solution to Example 7-2

Programmable Array Logic (PAL)

The programmable array logic (PAL) is a logic device with fixed OR array and a programmable AND array. It is easier to program but not as flexible as PLA.

Boolean functions must be simplified to fit into each section → product term cannot be shared among two or more gates.

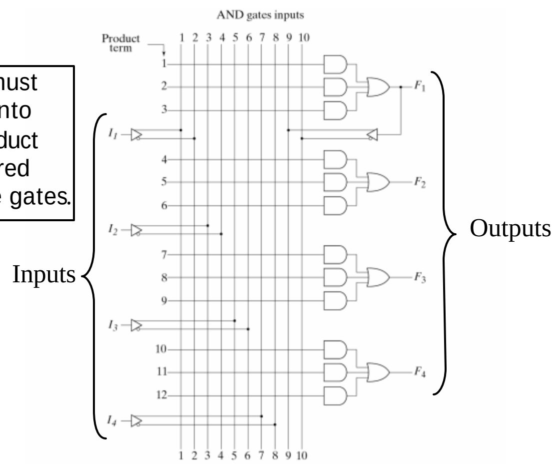


Fig. 7-16 PAL with Four Inputs, Four Outputs, and Three-Wide AND-OR Structure

Sequential Programmable Logic Devices

Simple or Sequential Programmable Logic Device (SPLD): Includes flip-flops and AND-OR array within the IC chip.

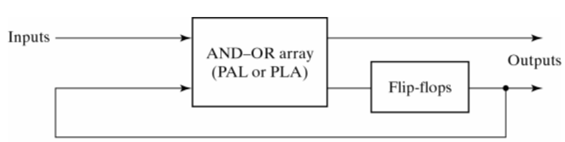


Fig. 7-18 Sequential Programmable Logic Device

Sequential Programmable Logic

A microcell is a section of a SPLD that contains a sum-of-product combinational logic and a flip-flop. A commercial SPLD contains 8 - 10 microcells in an IC package.

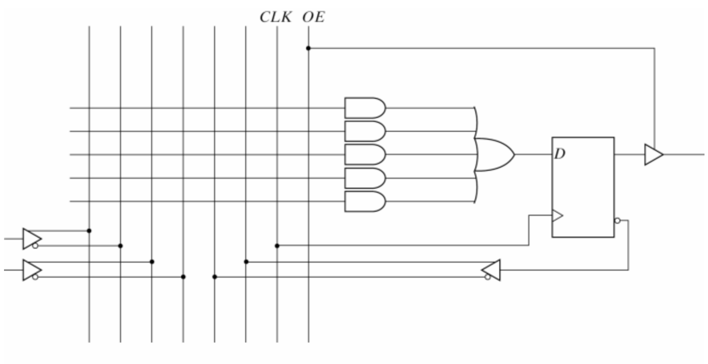


Fig. 7-19 Basic Macrocell Logic

Complex Programmable Logic Device (CPLD)

Complex Programmable Logic Device (CPLD):
The design of a complete digital system using PLD requires the use of several PLD's in a Complex Programmable Logic Device (CPLD) integrated on a single chip.

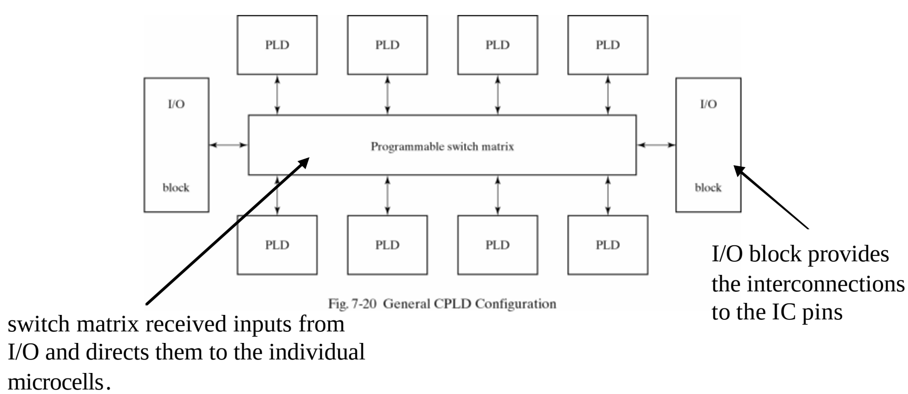


Fig. 7-20 General CPLD Configuration

Field-Programmable Gate Array (FPGA)

Field-Programmable Gate Array (FPGA): is a VLSI circuit whose function is defined by a user's program rather than by the manufacturer of the device (CPEN431)

• Depending on the particular device, the program is either 'burned' in permanently or semi-permanently as part of a board assembly process, or is loaded from an external memory each time the device is powered up.

• The Field-Programmable Gate Arrays provide the benefits of custom CMOS VLSI, while avoiding the initial cost and time delay.